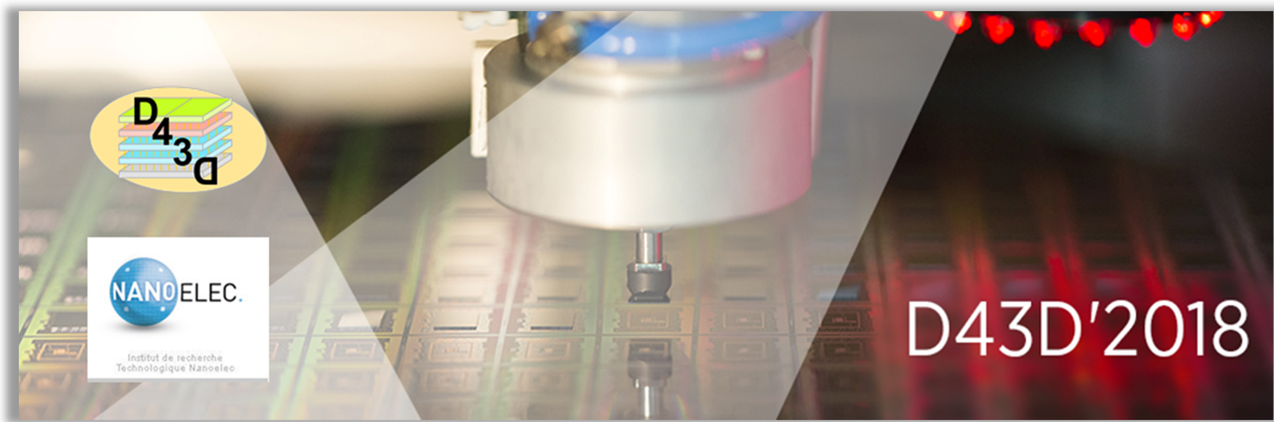

D43D WORKSHOP

2-3 July, 2018, Minatec, Grenoble

10th Workshop on Design for 3D Silicon Integration

Day 1, Monday, July 2nd, 2018		
13:00 - 14:30	**WELCOME LUNCH**	
14:30 - 14:35	**Opening Session**	**Pascal Vivet**, CEA-LETI, France
Session 1	**Advanced 3D Image Sensors with Smart Features**	
	Chair: Gilles Sicard, CEA-LETI, France	
14:35 - 15:00	**Direct Time-of-Flight (dTOF) imaging for depth sensing applications**	**Augusto Ronchini Ximenes**, TU Delft, Nederlands
15:00 - 15:30	**3D Architecture of a Fast Digital Burst Video Sensor**	**Wilfried Uhring**, Univ. Strasbourg, France
15:30 - 16:00	**RETINE: a 3D stacked in-focal-plane vision chip for monitoring applications**	**Laurent Millet**, CEA-LETI, France
16:00 - 16:30	**COFFEE BREAK**	
Session 2	**3D Integration Challenges for Photonics communication**	
	Chair : Alexis Farcy, STMicroelectronics, France	
16:30 - 16:50	**System-level Optimizations for 2.5D-integrated Chips with Silicon-Photonic Links**	**Ayse Coskun,** Univ. of Boston, USA
16:50 - 17:10	**Toward a Top-Down Synthesis Methodology for 3D-Stacked Wavelength-Routed Optical NoCs**	**Davide Bertozzi,** Univ. of Ferrara, Italy
17:10 - 17:30	**Laser Group Control for Efficient Thermal-Aware Calibration of Nanophotonic Interconnects**	**Ian O'Connor,** INL, France
17:30 - 17:50	**Face-to-face integration of an electro-optical link with CMOS drivers and thermal control**	**Yvain Thonnart,** CEA-LETI, France

Day 2, Tuesday, July 3rd, 2018		
8:30 - 9:00	**WELCOME COFFEE**	
Session 3	**3D Systems for Machine Learning and Memory architecture**	
	Chair : Subhasish Mitra, Stanford Univ., USA	
9:00 - 9:30	**3D Systems for Machine Learning**	**Paul Franzon**, Univ. of North Carolina, USA
9:30 - 10:00	**NTX: A Scalable Near-Memory Architecture for Training Deep Neural Networks on Large In-Memory Datasets**	**Luca Benini**, Univ. Bologna, Italy and ETH Zurich, Switzerland
10:00 - 10:30	**Challenges of 3D DRAM Memories**	**Christian Weis**, Univ. of Kaiserslautern, Germany
10:30 - 11:00	**COFFEE BREAK**	
Session 4	**3D Technology : Keynotes and Panel**	
	Chair : Severine Cheramy, CEA-LETI, Grenoble, France	
11:00 - 11:45	**3D scalability from high performance to ultra low power**	**Marcel Wieland**, Global Foundry, Germany
11:45 - 12:15	**3D Memory : trends and obstacles**	**Anton Korzh**, Micron, USA
12:15 - 13:00	**Panel** **"3D Technology : which road for which disruptive architectures ?"**	panelists : - **Subhasish Mitra**, Univ. Stanford, USA - **Paul Franzon**, NCSU, USA - **Marcel Wieland**, Global Foundry, Germany, - **Francois Jacquet**, KALRAY, France, - **Denis Dutoit**, CEA-LETI, France
13:00 - 14:30	**LUNCH BREAK**	
Session 5	**Monolithic 3D and advanced signalling**	
	Chair: Laurent Le-Pailleur, STMicroelectronics, France	
14:30 - 15:00	**3D sequential integration : review of opportunities and technology updates**	**Perrine Batude**, CEA-Leti, France
15:00 - 15:30	**3D sequential integration : overview of 65 nm on 28 nm FDSOI MPW architecture and design contributions**	**Sébastien Thuriès**, CEA-LETI, France
15:30 - 16:00	**Wireline Communication in 2.5-D and 3-D ICs**	**Przemyslaw Mroszczyk**, Univ. Manchester, UK
16:00 - 16:30	**COFFEE BREAK**	
Session 6	**3D Advanced Packaging and CAD tools**	
	Chair : Pascal Vivet, CEA-LETI, France	
16:30 - 16:55	**Solutions for high density advanced package design and verification**	**Pascal Leclaire**, Mentor Graphics, France
16:55 - 17:20	**From 2.5D to 3D layout design environment: Status and future challenges for advanced 3D packaging**	**Thomas Brandtner**, INFINEON, Austria
17:20 - 17:45	**CAD Flow methodologies for 3D Hybrid sub-systems**	**Lise Doyen**, STMicroelectronics, France